REMARKS

In response to the Office Action, dated November 23, 2001, the applicant hereby makes the following response. A Petition to Revive and a CPA were filed on May 18, 2001. The Petition to Revive was granted on June 28, 2001 while the CPA was treated an improper RCE . A Notice of Improper Request for RCE was issued on July 6, 2001. Accordingly, a Notice of Abandonment was issued on August 10, 2001. A Petition To Revive and an RCE were filed on October 23, 2001. The response filed in accordance with the RCE has not been acted upon.

Originally claims 1-9 were filed in which claims 1, 3, 5 and 7 were independent. In response to a restriction requirement claims 7-9 were withdrawn. In a response filed January 28, 2000 claims 1, 3 and 5 were amended and new claims 10-12 were added. In this response, claims 1, 3 and 5 are being amended, claim 4 is being cancelled and new claim 13-17 are being added. Applicants respectfully state that no new matter has been added.

Defective Oath or Declaration

Applicants respectfully note the Examiner's advisory action acknowledgment of the new declaration filed which correctly spells the inventor's name.

Rejection Under 35 U.S.C. § 102(e) and 103(c)

Pending Claims 1-6 and 10-12 stand rejected under 35 U.S.C. § 102(e) as being purportedly anticipated by *Ohsawa* (U.S. Patent No. 5,756,377) or, in the alternative, under 35 U.S.C. 103(a) as being purportedly obvious over *Ohsawa* (U.S. Patent No. 5,756,377). Claims 1, 3 and 5 have been amended, claim 4 has been cancelled and new claims 13-17 have been added. Applicants respectfully traverse the rejections and request withdrawal of same.

More importantly, the *Ohsawa* reference does not teach any sealing resin being filled in the through holes to increase the contact area between the sealing resin and the external ring to increase the bonding strength between the sealing resin and the external ring. Accordingly, the mechanical strength of the *Ohsawa* reference is not improved via the through holes. In the *Ohsawa* reference, a reinforcement plate is required to be adhered to the rear surface of the insulation film (See Column 3. Lines 1-5) to improve the device strength. Further, the *Ohsawa* reference does not teach an expanded open portion positioned on the inner circumference of the external ring (See specification page 19 , lines 13). Accordingly, the *Ohsawa* reference does not teach the angled open portion to allow a larger area between the semiconductor chip and the external ring.

To establish a prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art See In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Further, not only must the Examiner find each element of the claimed invention in the prior art, the Examiner must show upon "rigorous application" the proper motivation or suggestion to combine wherein the showing "must be clear and particular" See In re Dembiczak, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 17 (Fed. Cir. 1999).

The Applicants respectfully submit that the Examiner's limitation analysis fails to demonstrate how the reference teaches or suggests the combination to yield the claimed invention wherein the claimed invention has among other elements sealing resin filled in the through holes to increase the semiconductor device strength. In contrast, the reference is never concerned with this issues since the primary reference is designed with a hole and reinforcement plate and accordingly, do not discuss or enable the same issues to be solved.

The problem solved by the invention is to provide a more rigid and stable semiconductor device via the use of the through holes. Thus, the invention addresses a different problem and

proposes a much different solution from the problems and solutions in the art. See, In re Dembiczak, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999)(Evidence of a suggestion, teaching or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved)(Emphasis added).

The cited references is oriented to different problems and propose different solutions. In particular, the cited references do not suggest or teach sealing resin being filled in the through holes to increase the contact area between the chip and external ring. Accordingly, the present invention is superior over the references. Since the problems identified are different from the problem solved by the claimed invention, the claimed invention is not obvious.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be found in the prior art and not based on the applicants' disclosure.

Regarding the first criteria, the cited references do not provide any suggestion to modify the reference to obtain the claimed invention. Instead, the cited reference relates to different problems and proposes different solutions than the present invention. One skilled in the art would not be motivated to seek the *Ohsawa* reference since this reference requires a hole in the insulation layers to position the chip. In the present invention, the configuration does not allow for a hole to position the chip. Additionally, one skilled in the art would not be motivated to

seek the *Ohsawa* reference because the *Ohsawa* reference does not teach through holes that can be filled with the sealing resin to increase the contact area of the sealing resin.

Regarding the second criteria, the cited references do not provide a reasonable expectation of success. Other than applicants' disclosure, applicants are unaware of any prior uses of the claimed through holes of the external ring.

Finally, the cited references do not teach or suggest all the claim limitations of the present invention. The cited references do not teach the through holes or blind holes being filled with the sealing resin to increase the contact are between the sealing resin and external ring to improve the bonding strength between the chip and external ring.

In order to meet an obviousness requirement, the requirement has to meet some suggestion that the cited references have similar features or structures. To suggest otherwise pertains to an impermissible obvious to try standard. The standard, rather, is whether the reference taken as a whole would have suggested the applicant's invention to one of ordinary skill in the plasma display arts at the time the invention was made.

Therefore, Applicants respectfully submit that since Claims1, 3 and 5 are patentable, all dependent claims therefrom are also patentable.

CONCLUSION

In view of the foregoing, it is submitted that all of the pending claims are patentable. Further, the Examiner's rejections have been addressed herein. It is, therefore, submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

By its attorney,

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Date: 2/22, 2002

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2/22/02 JoEllen Hogan
Date JoEllen Hogan

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of: K. Ohsawa and H. Makino	)	
Serial No.: 09/009,248	)	Examiner: D. Graybill
Filed: January 20, 1998	)	Group Art Unit: 2814
For: LEAD FRAME AND SEMICONDUCTOR DEVICE HAVING THE SAME	)	

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Claims

1. (Twice Amended) A semiconductor device, comprising:

a semiconductor chip having a plurality of electrode pads formed at a periphery of a front surface thereof;

a wiring film formed on the front surface side of said semiconductor chip by laminating an insulation film on a lead pattern;

an outer connection terminal formed so as to protrude above said wiring film;

a plurality of leads extending from said wiring film and connected to the electrode pads on said semiconductor chip at extended tips end thereof;

an external ring provided so as to surround said semiconductor chip and formed with a plurality of through holes [or blind holes] positioned entirely outside of a perimeter edge of the semiconductor chip; and

a sealing resin filled between said semiconductor chip and said external ring, the sealing resin further being filled in the through holes to increase the contact area between the sealing

resin and the external ring which strengthens the bond between the sealing ring and the external ring.

3. (Twice Amended) A lead frame, comprising:

a wiring film formed by laminating an insulation film on a lead pattern;

an external connection terminal formed so as to protrude above said wiring film;

a plurality of leads extending from said wiring film and forming connecting portions to electrode pads on a semiconductor chip at extended tip ends thereof;

an external ring provided outside said wiring film, having an opening portion capable of housing said semiconductor chip and formed with a plurality of through holes [or blind holes] positioned entirely outside of a perimeter edge of the semiconductor chip when the opening portion houses the semiconductor chip wherein an outwardly extended open portion is formed on the opening portion and positioned on a rear surface side of the semiconductor chip.

5. (Twice Amended) An electronic apparatus including a printed wiring board loaded with a semiconductor chip, said semiconductor device, comprising:

a semiconductor chip having a plurality of electrode pads formed at a periphery of a front surface thereof;

a wiring film formed on a front surface side of said semiconductor chip by laminating an insulation film on lead patterns;

an outer connection terminal formed so as to protrude above said wiring film;

a plurality of leads extending from said wiring film and connected to the electrode pads on said semiconductor chip at extended tip ends thereof;

an external ring provided so as to surround said semiconductor chip and, formed with a plurality of through holes [or blind holes] positioned entirely outside of a perimeter edge of the semiconductor chip; and

a sealing resin filled between said semiconductor chip and said external ring, the sealing resin further being filled in the through holes to increase the contact area between the sealing resin and the external ring which strengthens the bond between the sealing ring and the external ring, wherein said external connection terminal and an electrode on said printed wiring board are connected.

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